

WEST[Help](#)[Logout](#)[Interrupt](#)[Main Menu](#)[Search Form](#)[Posting Counts](#)[Show S Numbers](#)[Edit S Numbers](#)[Preferences](#)[Cases](#)**Search Results -**

Term	Documents
"6044450"	1
6044450S	0
BRANCH	121887
BRANCHES	79783
LATENT	62899
LATENTS	27
LATENCY	18307
LATENCIES	3161
LATENCYS	0
WAIT	64105
WAITS	42508
(6044450.PN. AND BRANCH AND (DELAY\$3 OR LATENT OR LATENCY OR WAIT)).USPT.	1

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US Patents Full-Text Database
US Pre-Grant Publication Full-Text Database
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EPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Database:**Search:**

L5

[Refine Search](#)[Recall Text](#)[Clear](#)**Search History**

DATE: Wednesday, September 24, 2003 [Printable Copy](#) [Create Case](#)

Set Name Query

side by side

Hit Count Set Name

result set

*DB=USPT; PLUR=YES; OP=OR*L5 6044450.pn. and branch and (delay\$3 or latent or latency or wait)

1

L5*DB=USPT,PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=OR*L4 branch\$3 near5 (delay\$3 or wait or latenc\$3 or latent or nop or no
near1 operation or noop) near5 (field\$1 or portion\$1) near7
(extension\$ or extend\$3 or format or bit\$1 or byte\$1)

14

L4L3 branch\$3 near5 (delay\$3 or wait or latenc\$3 or latent or nop or no
near1 operation or noop) near5 (field\$1 or portion\$1)

105

L3L2 (delay\$3 or latent or latency or wait) near5 branch\$3 near8 target and
insert\$4 near5 (nop or no near1 operation or noop)

11

L2L1 (delay\$3 or latent or latency or wait) near5 branch\$3 near8 target

246

L1

END OF SEARCH HISTORY

WEST[Generate Collection](#)[Print](#)**Search Results - Record(s) 1 through 20 of 31 returned.**☐ 1. Document ID: US 20030169077 A1

L3: Entry 1 of 31

File: PGPB

Sep 11, 2003

PGPUB-DOCUMENT-NUMBER: 20030169077
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030169077 A1

TITLE: High-efficiency saturating operator

PUBLICATION-DATE: September 11, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Dupont De Dinechin, Benoit	Grenoble		FR	

US-CL-CURRENT: 326/104

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC
Draw	Desc	Image									

☐ 2. Document ID: US 20020065859 A1

L3: Entry 2 of 31

File: PGPB

May 30, 2002

PGPUB-DOCUMENT-NUMBER: 20020065859
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020065859 A1

TITLE: Devices and methods for estimating a series of symbols

PUBLICATION-DATE: May 30, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Le Bars, Philippe	Thorigne-Fouillard		FR	
Olier, Sylvain	Pluguffan		FR	

US-CL-CURRENT: 708/109

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC
Draw	Desc	Image									

☐ 3. Document ID: US 6539368 B1

L3: Entry 3 of 31

File: USPT

Mar 25, 2003

US-PAT-NO: 6539368

DOCUMENT-IDENTIFIER: US 6539368 B1

TITLE: Neural processor, saturation unit, calculation unit and adder circuit

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC
Draw Desc	Image										

☐ 4. Document ID: US 6529922 B1

L3: Entry 4 of 31

File: USPT

Mar 4, 2003

US-PAT-NO: 6529922

DOCUMENT-IDENTIFIER: US 6529922 B1

TITLE: Instruction set for controlling a processor to convert linear data to logarithmic data in a single instruction that define the exponent filed of the logarithmic value

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC
Draw Desc	Image										

☐ 5. Document ID: US 6298472 B1

L3: Entry 5 of 31

File: USPT

Oct 2, 2001

US-PAT-NO: 6298472

DOCUMENT-IDENTIFIER: US 6298472 B1

TITLE: Behavioral silicon construct architecture and mapping

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC
Draw Desc	Image										

☐ 6. Document ID: US 6237084 B1

L3: Entry 6 of 31

File: USPT

May 22, 2001

US-PAT-NO: 6237084

DOCUMENT-IDENTIFIER: US 6237084 B1

TITLE: Processor which can favorably execute a rounding process composed of positive conversion and saturated calculation processing

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KMC
Draw Desc	Image									

☐ 7. Document ID: US 6182105 B1

L3: Entry 7 of 31

File: USPT

Jan 30, 2001

US-PAT-NO: 6182105

DOCUMENT-IDENTIFIER: US 6182105 B1

TITLE: Multiple-operand addition with intermediate saturation

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

K/MC

☐ 8. Document ID: US 6112291 A

L3: Entry 8 of 31

File: USPT

Aug 29, 2000

US-PAT-NO: 6112291

DOCUMENT-IDENTIFIER: US 6112291 A

TITLE: Method and apparatus for performing a shift instruction with saturate by examination of an operand prior to shifting

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

K/MC

☐ 9. Document ID: US 6085275 A

L3: Entry 9 of 31

File: USPT

Jul 4, 2000

US-PAT-NO: 6085275

DOCUMENT-IDENTIFIER: US 6085275 A

**** See image for Certificate of Correction ****

TITLE: Data processing system and method thereof

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

K/MC

☐ 10. Document ID: US 6078940 A

L3: Entry 10 of 31

File: USPT

Jun 20, 2000

US-PAT-NO: 6078940

DOCUMENT-IDENTIFIER: US 6078940 A

TITLE: Microprocessor with an instruction for multiply and left shift with saturate

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

K/MC

☐ 11. Document ID: US 5974540 A

L3: Entry 11 of 31

File: USPT

Oct 26, 1999

US-PAT-NO: 5974540

DOCUMENT-IDENTIFIER: US 5974540 A

TITLE: Processor which can favorably execute a rounding process composed of positive conversion and saturated calculation processing

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMMC

☐ 12. Document ID: US 5930158 A

L3: Entry 12 of 31

File: USPT

Jul 27, 1999

US-PAT-NO: 5930158

DOCUMENT-IDENTIFIER: US 5930158 A

TITLE: Processor with instruction set for audio effects

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMMC

☐ 13. Document ID: US 5892696 A

L3: Entry 13 of 31

File: USPT

Apr 6, 1999

US-PAT-NO: 5892696

DOCUMENT-IDENTIFIER: US 5892696 A

TITLE: Pipeline controlled microprocessor

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMMC

☐ 14. Document ID: US 5847978 A

L3: Entry 14 of 31

File: USPT

Dec 8, 1998

US-PAT-NO: 5847978

DOCUMENT-IDENTIFIER: US 5847978 A

TITLE: Processor and control method for performing proper saturation operation

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMMC

☐ 15. Document ID: US 5805874 A

L3: Entry 15 of 31

File: USPT

Sep 8, 1998

US-PAT-NO: 5805874

DOCUMENT-IDENTIFIER: US 5805874 A

TITLE: Method and apparatus for performing a vector skip instruction in a data processor

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMIC

☐ 16. Document ID: US 5754805 A

L3: Entry 16 of 31

File: USPT

May 19, 1998

US-PAT-NO: 5754805

DOCUMENT-IDENTIFIER: US 5754805 A

TITLE: Instruction in a data processing system utilizing extension bits and method therefor

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMIC

☐ 17. Document ID: US 5752074 A

L3: Entry 17 of 31

File: USPT

May 12, 1998

US-PAT-NO: 5752074

DOCUMENT-IDENTIFIER: US 5752074 A

TITLE: Data processing system and method thereof

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMIC

☐ 18. Document ID: US 5742786 A

L3: Entry 18 of 31

File: USPT

Apr 21, 1998

US-PAT-NO: 5742786

DOCUMENT-IDENTIFIER: US 5742786 A

TITLE: Method and apparatus for storing vector data in multiple non-consecutive locations in a data processor using a mask value

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMIC

☐ 19. Document ID: US 5737586 A

L3: Entry 19 of 31

File: USPT

Apr 7, 1998

US-PAT-NO: 5737586

DOCUMENT-IDENTIFIER: US 5737586 A

TITLE: Data processing system and method thereof

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KVMC

☐ 20. Document ID: US 5734879 A

L3: Entry 20 of 31

File: USPT

Mar 31, 1998

US-PAT-NO: 5734879

DOCUMENT-IDENTIFIER: US 5734879 A

TITLE: Saturation instruction in a data processor

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KVMC

[Generate Collection](#)[Print](#)

Term	Documents
OPERAND\$1	0
OPERAND	20172
OPERANDA	15
OPERANDB	1
OPERANDE	2
OPERANDI	675
OPERANDL	5
OPERANDM	1
OPERANDN	1
OPERANDO	1
OPERANDS	15688
(L2 NEAR8 OPERAND\$1).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	31

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WEST[Generate Collection](#)[Print](#)**Search Results - Record(s) 21 through 31 of 31 returned.**☐ 21. Document ID: US 5751985 A

L2: Entry 21 of 31

File: USPT

May 12, 1998

US-PAT-NO: 5751985

DOCUMENT-IDENTIFIER: US 5751985 A

TITLE: Processor structure and method for tracking instruction status to maintain precise state

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC
Draw Desc	Image										

☒ 22. Document ID: US 5710912 A

L2: Entry 22 of 31

File: USPT

Jan 20, 1998

US-PAT-NO: 5710912

DOCUMENT-IDENTIFIER: US 5710912 A

TITLE: Method and apparatus for enabling a computer system to adjust for latency assumptions

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC
Draw Desc	Image										

☐ 23. Document ID: US 5673426 A

L2: Entry 23 of 31

File: USPT

Sep 30, 1997

US-PAT-NO: 5673426

DOCUMENT-IDENTIFIER: US 5673426 A

TITLE: Processor structure and method for tracking floating-point exceptions

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC
Draw Desc	Image										

☐ 24. Document ID: US 5673408 A

L2: Entry 24 of 31

File: USPT

Sep 30, 1997

US-PAT-NO: 5673408

DOCUMENT-IDENTIFIER: US 5673408 A

TITLE: Processor structure and method for renamable trap-stack

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC
Draw Desc	Image										

☐ 25. Document ID: US 5659721 A

L2: Entry 25 of 31

File: USPT

Aug 19, 1997

US-PAT-NO: 5659721

DOCUMENT-IDENTIFIER: US 5659721 A

TITLE: Processor structure and method for checkpointing instructions to maintain precise state

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC
Draw Desc	Image										

☐ 26. Document ID: US 5655115 A

L2: Entry 26 of 31

File: USPT

Aug 5, 1997

US-PAT-NO: 5655115

DOCUMENT-IDENTIFIER: US 5655115 A

TITLE: Processor structure and method for watchpoint of plural simultaneous unresolved branch evaluation

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Image									

☐ 27. Document ID: US 5651124 A

L2: Entry 27 of 31

File: USPT

Jul 22, 1997

US-PAT-NO: 5651124

DOCUMENT-IDENTIFIER: US 5651124 A

TITLE: Processor structure and method for aggressively scheduling long latency instructions including load/store instructions while maintaining precise state

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Image									

☐ 28. Document ID: US 5649136 A

L2: Entry 28 of 31

File: USPT

Jul 15, 1997

US-PAT-NO: 5649136

DOCUMENT-IDENTIFIER: US 5649136 A



TITLE: Processor structure and method for maintaining and restoring precise state at any instruction boundary

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KVMC

☐ 29. Document ID: US 5644742 A

L2: Entry 29 of 31

File: USPT

Jul 1, 1997

US-PAT-NO: 5644742

DOCUMENT-IDENTIFIER: US 5644742 A

TITLE: Processor structure and method for a time-out checkpoint

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KVMC

☐ 30. Document ID: US 5528898 A

L2: Entry 30 of 31

File: USPT

Jun 25, 1996

US-PAT-NO: 5528898

DOCUMENT-IDENTIFIER: US 5528898 A

TITLE: Apparatus for detecting deterioration of catalysts

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KVMC

☐ 31. Document ID: US 5333284 A

L2: Entry 31 of 31

File: USPT

Jul 26, 1994

US-PAT-NO: 5333284

DOCUMENT-IDENTIFIER: US 5333284 A

TITLE: Repeated ALU in pipelined processor design

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KVMC

[Generate Collection](#)[Print](#)

Term	Documents
LOAD	1314662
LOADS	295945
ARITHMETIC	162987
ARITHMETICS	410
ADD	671949
ADDS	230206
LATENT	138616
LATENTS	34
LATENCY	31902
LATENCIES	4862
LATENCY	1
(LOAD NEAR8 (ARITHMETIC OR ADD OR SUBTRACT\$3) NEAR8 (DELAY\$3 OR LATENT OR LATENCY OR WIAT) AND (NOP OR NO NEAR1 OPERATION)).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	31

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L2: Entry 1 of 31

File: PGPB

Sep 26, 2002

PGPUB-DOCUMENT-NUMBER: 20020138681

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020138681 A1

TITLE: Method of detecting a source strobe event using change detection

PUBLICATION-DATE: September 26, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Porterfield, A. Kent	New Brighton	MN	US	

US-CL-CURRENT: 710/305

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw	Desc	Image							

KMMC

☐ 2. Document ID: US 20020078325 A1

L2: Entry 2 of 31

File: PGPB

Jun 20, 2002

PGPUB-DOCUMENT-NUMBER: 20020078325

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020078325 A1

TITLE: Microcomputer and dividing circuit

PUBLICATION-DATE: June 20, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Kawasaki, Shumpei	Tokyo		JP	
Sakakibara, Eiji	Tokyo		JP	
Fukada, Kaoru	Tokyo		JP	
Yamazaki, Takanaga	Tokyo		JP	
Akao, Yasushi	Tokyo		JP	
Baba, Shiro	Tokyo		JP	
Kihara, Toshimasa	Tokyo		JP	
Kurakazu, Keiichi	Tokorozawa-shi		JP	
Tsukamoto, Takashi	Tokyo		JP	
Masumura, Shigeki	Tokyo		JP	
Tawara, Yasuhiro	Tokyo		JP	
Kashiwagi, Yugo	Tokyo		JP	
Fujita, Shuya	Tokyo		JP	
Ishida, Katsuhiko	Tokyo		JP	
Sawa, Noriko	Tokyo		JP	
Asano, Yoichi	Tokyo		JP	
Chaki, Hideaki	Tokorozawa-shi		JP	
Sugawara, Tadahiko	Tokyo		JP	
Kainaga, Masahiro	Yokohama-shi		JP	
Noguchi, Kouki	Tokyo		JP	
Watabe, Mitsuru	Naka-gun		JP	

US-CL-CURRENT: 712/210; 709/200

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KWC

☐ 3. Document ID: US 20020002670 A1

L2: Entry 3 of 31

File: PGPB

Jan 3, 2002

PGPUB-DOCUMENT-NUMBER: 20020002670

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020002670 A1

TITLE: DATA PROCESSING DEVICE

PUBLICATION-DATE: January 3, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
YOSHIDA, TOYOHIKO	TOKYO		JP	
FUJII, HIDEYUKI	TOKYO		JP	

US-CL-CURRENT: 712/245; 712/233

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KWC

☐ 4. Document ID: US 6598156 B1

L2: Entry 4 of 31

File: USPT

Jul 22, 2003

US-PAT-NO: 6598156

DOCUMENT-IDENTIFIER: US 6598156 B1

TITLE: Mechanism for handling failing load check instructions

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KMOC
Draw Desc	Image									

☐ 5. Document ID: US 6516462 B1

L2: Entry 5 of 31

File: USPT

Feb 4, 2003

US-PAT-NO: 6516462

DOCUMENT-IDENTIFIER: US 6516462 B1

TITLE: Cache miss saving for speculation load operation

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KMOC
Draw Desc	Image									

☐ 6. Document ID: US 6360315 B1

L2: Entry 6 of 31

File: USPT

Mar 19, 2002

US-PAT-NO: 6360315

DOCUMENT-IDENTIFIER: US 6360315 B1

TITLE: Method and apparatus that supports multiple assignment code

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KMOC
Draw Desc	Image									

☐ 7. Document ID: US 6343357 B1

L2: Entry 7 of 31

File: USPT

Jan 29, 2002

US-PAT-NO: 6343357

DOCUMENT-IDENTIFIER: US 6343357 B1

TITLE: Microcomputer and dividing circuit

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KMOC
Draw Desc	Image									

☐ 8. Document ID: US 6321330 B1

L2: Entry 8 of 31

File: USPT

Nov 20, 2001

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

[illegible]

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KNOIC
Draw Desc	Image									

[illegible]

☐ 16. Document ID: US 6000029 A

L2: Entry 16 of 31

File: USPT

Dec 7, 1999

US-PAT-NO: 6000029

DOCUMENT-IDENTIFIER: US 6000029 A

TITLE: Method and apparatus for affecting subsequent instruction processing in a data processor

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMC

☐ 17. Document ID: US 5991545 A

L2: Entry 17 of 31

File: USPT

Nov 23, 1999

US-PAT-NO: 5991545

DOCUMENT-IDENTIFIER: US 5991545 A

TITLE: Microcomputer having variable bit width area for displacement and circuit for handling immediate data larger than instruction word

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMC

☐ 18. Document ID: US 5969976 A

L2: Entry 18 of 31

File: USPT

Oct 19, 1999

US-PAT-NO: 5969976

DOCUMENT-IDENTIFIER: US 5969976 A

TITLE: Division circuit and the division method thereof

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMC

☐ 19. Document ID: US 5966530 A

L2: Entry 19 of 31

File: USPT

Oct 12, 1999

US-PAT-NO: 5966530

DOCUMENT-IDENTIFIER: US 5966530 A

TITLE: Structure and method for instruction boundary machine state restoration

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMC

☐ 20. Document ID: US 5941983 A

L2: Entry 20 of 31

File: USPT

Aug 24, 1999

US-PAT-NO: 5941983

DOCUMENT-IDENTIFIER: US 5941983 A

TITLE: Out-of-order execution using encoded dependencies between instructions in queues to determine stall values that control issuance of instructions from the queues

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KWC

[Generate Collection](#)[Print](#)

Term	Documents
LOAD	1314662
LOADS	295945
ARITHMETIC	162987
ARITHMETICS	410
ADD	671949
ADDS	230206
LATENT	138616
LATENTS	34
LATENCY	31902
LATENCIES	4862
LATENCYS	1
(LOAD NEAR8 (ARITHMETIC OR ADD OR SUBTRACT\$3) NEAR8 (DELAY\$3 OR LATENT OR LATENCY OR WIAT) AND (NOP OR NO NEAR1 OPERATION)).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	31

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WEST[Generate Collection](#)[Print](#)**Search Results - Record(s) 1 through 9 of 9 returned.**☒ 1. Document ID: US 6499096 B1

L7: Entry 1 of 9

File: USPT

Dec 24, 2002

US-PAT-NO: 6499096

DOCUMENT-IDENTIFIER: US 6499096 B1

TITLE: VLIW processor for exchanging and inputting sub-instructions to containers,
and code compression device and method for compressing program code

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC
Draw Desc	Image										

☐ 2. Document ID: US 6308261 B1

L7: Entry 2 of 9

File: USPT

Oct 23, 2001

US-PAT-NO: 6308261

DOCUMENT-IDENTIFIER: US 6308261 B1

TITLE: Computer system having an instruction for probing memory latency

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC
Draw Desc	Image										

☐ 3. Document ID: US 6234003 B1

L7: Entry 3 of 9

File: USPT

May 22, 2001

US-PAT-NO: 6234003

DOCUMENT-IDENTIFIER: US 6234003 B1

TITLE: Method of judging the lip turnover of a seal and apparatus for inserting a
seal

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC
Draw Desc	Image										

☒ 4. Document ID: US 5958044 A

L7: Entry 4 of 9

File: USPT

Sep 28, 1999

US-PAT-NO: 5958044

DOCUMENT-IDENTIFIER: US 5958044 A

TITLE: Multicycle NOP

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC
Draw Desc	Image										

☐ 5. Document ID: US 5850552 A

L7: Entry 5 of 9

File: USPT

Dec 15, 1998

US-PAT-NO: 5850552

DOCUMENT-IDENTIFIER: US 5850552 A

TITLE: Optimization apparatus for removing hazards by arranging instruction order

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC
Draw Desc	Image										

☒ 6. Document ID: US 5163139 A

L7: Entry 6 of 9

File: USPT

Nov 10, 1992

US-PAT-NO: 5163139

DOCUMENT-IDENTIFIER: US 5163139 A

TITLE: Instruction preprocessor for conditionally combining short memory instructions into virtual long instructions

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC
Draw Desc	Image										

☐ 7. Document ID: US 4972359 A

L7: Entry 7 of 9

File: USPT

Nov 20, 1990

US-PAT-NO: 4972359

DOCUMENT-IDENTIFIER: US 4972359 A

**** See image for Certificate of Correction ****

TITLE: Digital image processing system

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments		KWIC
Draw Desc	Image										

☐ 8. Document ID: US 4967349 A

L7: Entry 8 of 9

File: USPT

Oct 30, 1990

US-PAT-NO: 4967349

DOCUMENT-IDENTIFIER: US 4967349 A

TITLE: Digital signal processor suitable for extracting minimum and maximum values at

high speed

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMC

☐ 9. Document ID: US 4485650 A

L7: Entry 9 of 9

File: USPT

Dec 4, 1984

US-PAT-NO: 4485650

DOCUMENT-IDENTIFIER: US 4485650 A

TITLE: Method of measuring the normalized magnitude of ring opening in spiral pipe

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
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DB=USPT; PLUR=YES; OP=OR

<u>L7</u>	load near10 (arithmetic or add or subtract\$3) near10 (delay\$3 or latent or latency or wait or no near1 operation or nop or noop) near5 (insert\$4 or field\$1 or cod\$3 or defin\$4 or format\$4)	9	<u>L7</u>
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<u>L6</u>	load near10 (arithmetic or add or subtract\$3) near10 (delay\$3 or latent or latency or wait or no near1 operation or nop or noop) near5 (insert\$4 or field\$1 or cod\$3 or defin\$4 or format\$4)	0	<u>L6</u>
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DB=USPT,PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=OR

<u>L5</u>	load near10 (arithmetic or add or subtract\$3) near10 (delay\$3 or latent or latency or wait) and (nop or no near1 operation) near5 (insert\$4 or field\$1)	13	<u>L5</u>
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DB=USPT; PLUR=YES; OP=OR

<u>L4</u>	L3 not l2	0	<u>L4</u>
<u>L3</u>	load near10 (arithmetic or add or subtract\$3) near10 (delay\$3 or latent or latency or wiat) and (nop or no near1 operation) near5 insert\$4	12	<u>L3</u>

DB=USPT,PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=OR

<u>L2</u>	load near8 (arithmetic or add or subtract\$3) near8 (delay\$3 or latent or latency or wiat) and (nop or no near1 operation)	31	<u>L2</u>
<u>L1</u>	load near8 (arithmetic or add or subtract\$3) near8 (delay\$3 or latent or latency or wiat)	203	<u>L1</u>

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Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWMC
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☐ 3. Document ID: US 20010003822 A1

L2: Entry 3 of 11

File: PGPB

Jun 14, 2001

PGPUB-DOCUMENT-NUMBER: 20010003822
PGPUB-FILING-TYPE: new-utility
DOCUMENT-IDENTIFIER: US 20010003822 A1

TITLE: BINARY PROGRAM CONVERSION APPARATUS, BINARY PROGRAM CONVERSION METHOD AND
PROGRAM RECORDING MEDIUM

PUBLICATION-DATE: June 14, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
HIBI, YOSHINOBU	KAWASAKI-SHI		JP	
NISHI, HIDEFUMI	KAWASAKI-SHI		JP	
IZUCHI, TOSHIKI	KAWASAKI-SHI		JP	
KITAOKA, MASA HARU	KAWASAKI-SHI		JP	

US-CL-CURRENT: 709/100

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
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☒ 4. Document ID: US 6591414 B2

L2: Entry 4 of 11

File: USPT

Jul 8, 2003

US-PAT-NO: 6591414
DOCUMENT-IDENTIFIER: US 6591414 B2

TITLE: Binary program conversion apparatus, binary program conversion method and
program recording medium

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Image									

☒ 5. Document ID: US 6157988 A

L2: Entry 5 of 11

File: USPT

Dec 5, 2000

US-PAT-NO: 6157988
DOCUMENT-IDENTIFIER: US 6157988 A

TITLE: Method and apparatus for high performance branching in pipelined microsystems

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Image									

☐ 6. Document ID: US 5958044 A

L2: Entry 6 of 11

File: USPT

Sep 28, 1999

US-PAT-NO: 5958044

DOCUMENT-IDENTIFIER: US 5958044 A

TITLE: Multicycle NOP

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KMC
Draw Desc	Image									

☐ 7. Document ID: US 5809294 A

L2: Entry 7 of 11

File: USPT

Sep 15, 1998

US-PAT-NO: 5809294

DOCUMENT-IDENTIFIER: US 5809294 A

TITLE: Parallel processing unit which processes branch instructions without decreased performance when a branch is taken

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KMC
Draw Desc	Image									

☐ 8. Document ID: US 5774709 A

L2: Entry 8 of 11

File: USPT

Jun 30, 1998

US-PAT-NO: 5774709

DOCUMENT-IDENTIFIER: US 5774709 A

TITLE: Enhanced branch delay slot handling with single exception program counter

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KMC
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☒ 9. Document ID: US 5590294 A

L2: Entry 9 of 11

File: USPT

Dec 31, 1996

US-PAT-NO: 5590294

DOCUMENT-IDENTIFIER: US 5590294 A

**** See image for Certificate of Correction ****

TITLE: Method and apparatus for retarting pipeline processing

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KMC
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☐ 10. Document ID: US 5142634 A

L2: Entry 10 of 11

File: USPT

Aug 25, 1992

US-PAT-NO: 5142634

DOCUMENT-IDENTIFIER: US 5142634 A

TITLE: Branch prediction

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
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☐ 11. Document ID: JP 06274352 A

L2: Entry 11 of 11

File: JPAB

Sep 30, 1994

PUB-NO: JP406274352A

DOCUMENT-IDENTIFIER: JP 06274352 A

TITLE: COMPILER AND DATA PROCESSOR

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
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LATENTS	34
LATENCY	31902
LATENCIES	4862
LATENCYS	1
WAIT	97735
WAITS	59677
TARGET	509665
TARGETS	86139
NOP	4286
NOPS	404
((DELAY\$3 OR LATENT OR LATENCY OR WAIT) NEAR5 BRANCH\$3 NEAR8 TARGET AND INSERT\$4 NEAR5 (NOP OR NO NEAR1 OPERATION OR NOOP)).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	11

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result set

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<u>L4</u>	branch\$3 near5 (delay\$3 or wait or latenc\$3 or latent or nop or no near1 operation or noop) near5 (field\$1 or portion\$1) near7 (extension\$ or extend\$3 or format or bit\$1 or byte\$1)	14	<u>L4</u>
<u>L3</u>	branch\$3 near5 (delay\$3 or wait or latenc\$3 or latent or nop or no near1 operation or noop) near5 (field\$1 or portion\$1)	105	<u>L3</u>
<u>L2</u>	(delay\$3 or latent or latency or wait) near5 branch\$3 near8 target and insert\$4 near5 (nop or no near1 operation or noop)	11	<u>L2</u>
<u>L1</u>	(delay\$3 or latent or latency or wait) near5 branch\$3 near8 target	246	<u>L1</u>

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